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EXAMINER	
KIM, DAVID S	

ART UNIT	PAPER NUMBER
2613	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/767,376	DIAZ, NELSON	
	Examiner	**Art Unit**	
	DAVID S. KIM	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _01 July 2008_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-17_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-17_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunst et al. (U.S. Patent No. 6,934,470 B1, hereinafter "Kunst") in view of Knudsen (U.S. Patent No. 6,373,423 B1, hereinafter "Knudsen"), with reference to Weik (*Fiber Optics Standard Dictionary, 3rd ed.*).

Regarding claim 1, Kunst, with reference to Weik, discloses:

A receiver in a fiber optic system configured to receive an optical signal of varying light intensity and to produce a data output signal proportional thereto, the receiver comprising:

an optical detector (106 in Fig. 1) configured to receive the optical signal, the optical detector having a dynamic range of sensitivity between a high optical intensity value and a low optical intensity value (photodiodes operate in limited ranges), the optical detector further configured to convert the received optical signal into an analog electrical signal proportional to the optical intensity of the optical signal ("proportional" in col. 1, l. 24-28);

an electronic circuit (e.g., 112 in Fig. 1) coupled to the optical detector, the electronic circuit configured to receive the analog electrical signal from the optical detector and to produce digital data (the output of 112 in Fig. 1 of Kunst is a "representation…to which meaning is assigned", as described by Weik, "data" on p. 185) signals representative of the optical intensity of the optical signal (notice the analog to digital conversion of converter 112) such that the electronic circuit is configured to have an original maximum digital value proportional to the high optical intensity value and an original minimum digital value proportional to the low optical intensity value ("proportional" in col. 1, l. 24-28) thereby defining an original receiver resolution between the original minimum and maximum digital values (e.g., resolution of 14 or 7 bits), and the electronic circuit further being configured such that a relative magnitude

of the optical signal ("magnitude" in col. 1, l. 34) is represented at various points in time (the apparatus of Kunst operates in time) by a discrete number of digital values as an intelligent signal that comprises an output of the electronic circuit (N-bit digital output from 112).

Kunst, with reference to Weik, does not expressly disclose:

an adjustment circuit coupled to the electronic circuit in parallel with the optical detector and configured to allow the original maximum digital value to be adjusted to an adjusted maximum digital value, the adjusted maximum digital value determined by a maximum value of the analog electrical signal and to allow the original minimum digital value to be adjusted to an adjusted minimum digital value, the adjusted minimum digital value determined by a minimum value of the analog electrical signal, thereby defining an adjusted receiver resolution between the adjusted minimum and maximum digital values.

However, such adjustment circuits are known in the art. Knudsen shows one example of such a circuit, e.g., circuitry 415 and 210D in Fig. 4. Consider the following characterization of the teachings of Knudsen.

Regarding the "parallel" limitation, notice the "parallel" coupling to the side of input 105.

Regarding the "digital" value limitation, the voltage values of the sliding voltage range window correspond to "digital" values, e.g., col. 8, l. 28-40.

Regarding the "original maximum digital value" and "original minimum digital value" limitations, one may characterize the end values of the original sliding voltage range window of col. 7, l. 49-53 as a "maximum" value and a "minimum" value, and so they would correspond to the "original maximum digital value" and the "original minimum digital value".

Regarding the "adjusted maximum digital value" and the "adjusted minimum digital value" limitations, this sliding voltage range window is adjusted in col. 7, l. 49-53, and such adjustment implies adjusted end values of this adjusted sliding voltage range window. One may characterize the end values of this adjusted sliding voltage range window as a "maximum" value and a "minimum" value, and so they would correspond to the "adjusted maximum digital value" and the "adjusted minimum digital value".

Regarding the "determined by a maximum value of the analog electrical signal" and the "determined by a minimum value of the analog electrical signal" limitations, notice input analog signal 105 in Fig. 4. Also, notice the input to 415 in Fig. 4. This input to 415 is used to provide an indication of a voltage, i.e., values of the analog electrical signal, to expect as the input 105, col. 11, l. 1-13. These indications of voltage, i.e., values of the analog electrical signal, are used in a feedforward method for adjusting the sliding voltage range window, col. 10, l. 62. As the general purpose of this sliding voltage range window is to ensure that the input analog signal 105 falls within the voltage range window, col. 7, l. 49-53, it follows that the indications of voltage, i.e., values of the analog electrical signal, are used to determine the end values of the adjusted sliding voltage range window, i.e., the "adjusted maximum digital value" and the "adjusted minimum digital value". Since the end values of the adjusted sliding voltage range window, i.e., the "adjusted maximum digital value" and the "adjusted minimum digital value", are adjusted to ensure that the input analog signal 105 falls within the voltage range window, col. 7, l. 49-53, it follows that, at the time the invention was made, it would have been obvious to one of ordinary skill in the art to select end values that would fit the limits of the input analog electrical signal, i.e., the "maximum" and "minimum" values of the input analog electrical signal. One of ordinary skill in the art would have been motivated to do this to accurately capture the entirety of the input analog electrical signal. Otherwise, these values of the analog electrical signal would not be accurately captured, resulting in loss of accurate signal information.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to implement the adjustment circuit (analog-to-digital (A/D)) teachings of Knudsen in the converter 112 of Kunst, which includes A/D circuitry. One of ordinary skill in the art would have been motivated to do this for various benefits: reduced chip space and power requirements, reduced noise, reduced capacitance problems (Knudsen, col. 2, l. 59-61, relative to other possible prior art A/D converter embodiments, e.g., Fig. 1, col. 1, l. 16 - col. 2, l. 61) and greater resolution (Knudsen, col. 8, l. 24-25).

Regarding claim 2, Kunst, with reference to Weik, in view of Knudsen discloses:

The receiver of claim 1 wherein the adjusted maximum digital value is different than the original maximum digital value (Knudsen, sliding window in Fig. 3B).

Regarding claim 3, Kunst, with reference to Weik, in view of Knudsen discloses:

The receiver of claim 1 wherein the adjusted minimum digital value is different than the original minimum digital value (Knudsen, sliding window in Fig. 3B).

Regarding claim 4, Kunst, with reference to Weik, in view of Knudsen discloses:

The receiver of claim 1 wherein the adjusted maximum digital value is lower than the original maximum digital value and the adjusted minimum digital value is higher than the original minimum digital value (Knudsen, sliding window in Fig. 3B) such that the adjusted receiver resolution is finer than the original receiver resolution (Knudsen, col. 8, l. 24-25).

Regarding claim 5, Kunst, with reference to Weik, in view of Knudsen discloses:

The receiver of claim 1 wherein the adjusted maximum digital value is proportional to a highest anticipated optical value for the optical signal received by the optical detector and wherein the adjusted minimum digital value is proportional to a lowest anticipated optical value of the optical signal received by the optical detector (the output is proportional in col. 1, l. 16-28 of Kunst and the range values of Knudsen would be set to fit this output, col. 7, l. 49-53, so the range values would be proportional).

Regarding claim 6, Kunst, with reference to Weik, in view of Knudsen discloses:

The receiver of claim 1 wherein the adjusted maximum digital value is less than the original maximum digital value and is proportional to a highest anticipated optical value for the optical signal received by the optical detector and wherein the adjusted minimum digital value is higher than the original minimum digital value is proportional to a lowest anticipated optical value of the optical signal received by the optical detector (Knudsen, sliding window in Fig. 3B; the output is proportional in col. 1, l. 16-28 of Kunst and the range values of Knudsen would be set to fit this output, col. 7, l. 49-53, so the range values would be proportional).

Regarding claim 7, Kunst, with reference to Weik, in view of Knudsen discloses:

The receiver of claim 1 wherein the dynamic range of sensitivity is between a high optical intensity value of positive 7 dBm and a low optical intensity value of negative 20 dBm (Kunst, corresponding range in Watts in col. 1, l. 29-32).

Regarding claim 8, Kunst, with reference to Weik, in view of Knudsen discloses:

The receiver of claim 1 wherein the electronic circuit includes an analog-to-digital converter (Kunst, converter 112 in Fig. 1 includes analog-to-digital (A/D) circuitry) configured to receive the analog electrical signal and to convert the electrical signal into digital signals.

Regarding claim 9, Kunst, with reference to Weik, in view of Knudsen discloses:

The receiver of claim 8 wherein the analog-to-digital converter converts the analog electrical signal into a series of 8-bit digital values (Knudsen, notice the variable number of bits in col. 8, l. 30-32).

Regarding claim 10, Kunst, with reference to Weik, in view of Knudsen discloses:

The receiver of claim 9 wherein the lowest 8-bit digital value is originally the original minimum digital value (Knudsen, Fig. 3B, the lowest value could correspond to ground 112) and then adjusted to the adjusted minimum digital value (Knudsen, Fig. 3B, the sliding lower bound 212B), and wherein the highest 8-bit digital value is originally the original maximum digital value (Knudsen, Fig. 3B, the lowest value could correspond to maximum reference voltage 380B) and then adjusted to the adjusted maximum digital value (Knudsen, Fig. 3B, the sliding upper bound 212A).

Regarding claim 11, Kunst, with reference to Weik, in view of Knudsen does not expressly disclose:

The receiver of claim 1 assembled into a intelligent small form factor pluggable module for use with a fiber optic system.

However, Examiner takes Official Notice that such form factor pluggable modules are known in the art. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to assemble the receiver of Kunst, with reference to Weik, in view of Knudsen into one of these modules. One of ordinary skill in the art would have been motivated to do this for at least the benefit of compact size.

3. **Claims 12-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunst et al. in view of Knudsen, as applied to the claims above, and further in view of Yoo et al. (“A power and resolution adaptive flash analog-to-digital converter”, hereinafter “Yoo”).

Regarding claim 12, Kunst in view of Knudsen discloses:

A fiber optic communication system comprising:

a signal transmitter (Kunst, Fig. 1, implied source of transmitted signals into fiber 102) that produces optical signals of varying light intensity;

an optical fiber (Kunst, Fig. 1, fiber 102) coupled to the signal transmitter that receives and transmits the optical signals;

a receiver (Kunst, Fig. 1, receiving end) coupled to the optical fiber that receives the optical signals and produces a data signal proportional thereto, the receiver further comprising:

an optical detector (Kunst, 106) configured to receive the optical signals, the optical detector having a dynamic range of sensitivity between a high optical value and a low optical value (photodiodes operate in limited ranges), the optical detector further configured to convert the received optical signals into electrical signals proportional to the optical intensity of the optical signals (Kunst, "proportional" in col. 1, l. 24-28);

an electronic circuit (Kunst, 112) coupled to the optical detector, the electronic circuit configured to receive the electrical signals from the optical detector and to have an initial digital range (Kunst, notice the analog to digital conversion of converter 112) representative of the dynamic range, the initial digital range being defined between an initial maximum digital value and an initial minimum digital value (Kunst, "range" in col. 1, l. 36-42), the initial maximum digital value being proportional to high optical value and the initial minimum digital value being proportional to low optical value (Kunst, "proportional" in col. 1, l. 24-28); and

an adjustment circuit (converter 112 of Kunst in view of the A/D teachings of Knudsen, see the treatment of claim 1 above) coupled to the electronic circuit configured to allow the initial maximum digital value (see the treatment of "original maximum digital value" in claim 1 above) to be adjusted to an adjusted maximum digital value (see the treatment of "adjusted maximum digital value" in claim 1 above) and to allow the initial minimum digital value (see the treatment of "original minimum digital value" in claim 1 above) to be adjusted to an adjusted minimum digital value (see the treatment of "adjusted minimum digital value" in claim 1 above) thereby defining an adjusted digital range (Knudsen, sliding window in Fig. 3B), the adjusted maximum digital value being proportional to a highest anticipated optical value and the adjusted minimum digital value

being proportional to a lowest anticipated optical value (the output is proportional in col. 1, l. 16-28 of Kunst and the range values of Knudsen would be set to fit this output, col. 7, l. 49-53, so the range values would be proportional).

Kunst in view of Knudsen does not expressly disclose:

wherein a number of steps of resolution between the adjusted minimum and maximum digital values is greater than a number of steps of resolution between the initial minimum and maximum digital values.

However, such a concept is known in the art, as exemplified by Yoo (p. 233, col. 2, last paragraph, the examples of the resolution reduction and increase). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to implement this known concept in the apparatus of the prior art of record. One of ordinary skill in the art would have been motivated to do this to have increased resolution when receiving a weak signal (Yoo, p. 233, col. 2, last paragraph, the example of the resolution increase). Otherwise, details of the weak signal may not be detected due to an insufficient level of resolution.

Regarding claim 13, Kunst in view of Knudsen and Yoo discloses:

The fiber optic communication system of claim 12 wherein the adjusted maximum digital value is different than the initial maximum digital value (Knudsen, sliding window in Fig. 3B).

Regarding claim 14, Kunst in view of Knudsen and Yoo discloses:

The fiber optic communication system of claim 12 wherein the adjusted maximum digital value is lower than the initial maximum digital value and the adjusted minimum digital value is higher than the initial minimum digital value (Knudsen, sliding window in Fig. 3B) such that the adjusted digital range has more resolution (Knudsen, col. 8, l. 24-25) than the initial digital range.

Regarding claim 15, Kunst in view of Knudsen and Yoo discloses:

The fiber optic communication system of claim 12 wherein the electronic circuit includes an analog-to-digital converter (Kunst, converter 112 in Fig. 1) configured to receive the analog electrical signal and to convert the electrical signal into a digital signal.

Regarding claim 16, Kunst in view of Knudsen and Yoo does not expressly disclose:

The fiber optic communication system of claim 12 wherein the receiver is assembled into an intelligent small form factor pluggable module for use in the fiber optic system.

However, Examiner takes Official Notice that such form factor pluggable modules are known in the art. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to assemble the receiver of Kunst in view of Knudsen and Yoo into one of these modules. One of ordinary skill in the art would have been motivated to do this for at least the benefit of compact size.

Regarding claim 17, Kunst in view of Knudsen and Yoo discloses:

A receiver in a fiber optic system, the receiver comprising:

an optical detector (Kunst, 106) configured to receive an optical signal of varying light intensity, the optical detector having a dynamic range of sensitivity between a high optical intensity value and a low optical intensity value (photodiodes operate in limited ranges), the optical detector further configured to convert the received optical signal into an analog electrical signal proportional to the optical intensity of the optical signal (Kunst, “proportional” in col. 1, l. 24-28);

an electronic circuit (Kunst, 112) coupled to the optical detector, the electronic circuit configured to receive the analog electrical signal from the optical detector and to produce digital signals (Kunst, notice the analog to digital conversion of converter 112) representative of the optical intensity of the optical signal such that the electronic circuit is configured with an original maximum digital value proportional to the high optical intensity value and an original minimum digital value proportional to the low optical intensity value (Kunst, “proportional” in col. 1, l. 24-28) thereby defining an original receiver resolution between the original minimum and maximum digital values (Kunst, e.g., resolution of 14 or 7 bits); and

adjustment means (converter 112 of Kunst in view of the A/D teachings of Knudsen, see the treatment of claim 1 above) coupled to the electronic circuit for adjusting the original maximum digital

value (see the treatment of “original maximum digital value” in claim 1 above) to an adjusted maximum digital value (see the treatment of “adjusted maximum digital value” in claim 1 above) and for adjusting the original minimum digital value (see the treatment of “original minimum digital value” in claim 1 above) to an adjusted minimum digital value (see the treatment of “adjusted minimum digital value” in claim 1 above) thereby defining an adjusted receiver resolution (Knudsen, sliding window in Fig. 3B) between the adjusted minimum and maximum digital values, wherein the adjusted maximum digital value and the adjusted minimum value are selected based on an anticipated minimum and maximum values of the analog electrical signal (see the treatment of “determined by a maximum value of the analog electrical signal” and the “determined by a minimum value of the analog electrical signal” in claim 1 above)<u>, and wherein the adjustment means is operable to adjust both a relative number of steps of resolution (reduced or increased resolution of Yoo, p. 233, col. 2, last paragraph, through the number of steps of resolution of Kunst, N bits of 112 in Fig. 1, or Knudsen, N bits in Fig. 4), as well as a relative width of steps of resolution (Knudsen, change in the “width” in col. 8, l. 13-14)</u>.

<u>Response to Arguments</u>

4. Applicant's arguments filed on 01 July 2008, regarding **claim 1**, have been fully considered but they are not persuasive. Applicant states:

> **A. Claim 1**
> By this paper, claim 1 has been amended herein to recite "...the electronic circuit further being configured such that a relative magnitude of the optical signal is represented at various points in time by a discrete number of digital values as an intelligent signal that comprises an output of the electronic circuit; ..." Support for this amendment can be found throughout the application, including at page 7, lines 1-15. In contrast, the Examiner has not shown that the references, considered singly or in combination, teach or suggest this element in combination with the other elements of claim 1.
> In view of the foregoing, Applicant respectfully submits that the Examiner has failed to establish a prima facie case of obviousness with respect to claim 1 at least because the Examiner has not shown that there is any suggestion or motivation to make the purportedly obvious combination, and because the Examiner has not shown that the references, when combined in the purportedly obvious fashion, teach or suggest all the elements of claim 1. Applicant thus submits that the rejection of claim 1, as well as the rejection of dependent claims 2-11 (which each require all the elements of claim 1), should be withdrawn.
>
> (REMARKS, p. 8, section A).

Examiner respectfully points out the claim mapping provided for this limitation, detailed in the treatment of claim 1 above. Accordingly, this point is not persuasive.

5. Applicant's arguments with filed on 01 July 2008, regarding **claims 12 and 17**, have been considered but are moot in view of the new ground(s) of rejection. In particular, Applicant's arguments (REMARKS, p. 9, sections B and C) are based on newly introduced limitations to amended claims 12 and 17. Notice that the standing rejections address these teachings in view of the newly discovered teachings of Yoo.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hales (U.S. Patent Application Publication No. 2004/0001018 A1) is cited to show the increase of the resolution of an analog-to-digital converter by increasing the number of steps of resolution and by adjusting a relative width of steps of resolution (Figs. 8 and 9).

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID S. KIM whose telephone number is (571)272-3033. The examiner can normally be reached on Mon.-Fri. 9 AM to 5 PM (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth N. Vanderpuye can be reached on 571-272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. S. K./
Examiner, Art Unit 2613

/Kenneth N Vanderpuye/
Supervisory Patent Examiner, Art Unit 2613